IN THE CLAIMS

Please amend the claims by adding claims 31-40 as shown below.

1. - 2. (Canceled)

3. (Previously Presented) A processor comprising:

an execution pipeline having a register renaming stage to rotate registers in software pipelined loops;

a register rotation prediction unit connected to the register renaming stage to predict register addresses for future loop iterations;

a software pipeline instruction buffer to hold buffered instructions with predicted register addresses; and

unarchitected predicate registers connected to the execution pipeline and register prediction unit and operable to predicate the buffered instructions.

4. (Previously Presented) A processor comprising:

an execution pipeline having a register renaming stage to rotate registers in software pipelined loops;

a register rotation prediction unit connected to the register renaming stage to predict register addresses for future loop iterations;

a buffer to hold buffered instructions with predicted register addresses; and

the predicted register addresses allow the buffered instructions to be issued simultaneously with a branch instruction.

5. (Previously Presented) A processor comprising:

an execution pipeline having a register renaming stage to rotate registers in software pipelined loops;

a register rotation prediction unit to predict register addresses for future loop iterations; and

a hint register to encode prediction hints for the register rotation prediction unit.

6. (Previously Presented) The processor of claim 5 wherein the hint register is configured to hold static hints generated by a compiler.

7. (Original) The processor of claim 5 wherein the hint register is configured to hold dynamic hints generated at runtime.

8. (Original) The processor of claim 5 wherein the hint register is configured to hold an iteration distance.

9. (Previously Presented) A processor comprising:

an execution pipeline having a register renaming stage to rotate registers in software pipelined loops;

a register rotation prediction unit connected to the register renaming stage to predict register addresses for future loop iterations; and

a plurality of unarchitected frame marker registers connected to the execution pipeline and the register rotation prediction unit.

10. (Original) The processor of claim 9 wherein the register rotation prediction unit comprises speculation decision making hardware to compute values for the plurality of unarchitected frame marker registers.

11. (Original) The processor of claim 10 further comprising register renaming hardware in a pipeline, the register renaming hardware being responsive to the plurality of unarchitected frame marker registers.

12. (Previously Presented) The processor of claim 5 further comprising a trace cache.

13. (Previously Presented) The processor of claim 12 wherein the trace is configured to hold a prediction hint information for each trace.

14. (Original) The processor of claim 13 further comprising a trace cache fill unit to apply register rotation prediction to traces as traces are constructed.

15. (Canceled)

16. (Canceled)

17. (Previously Presented) A processing system comprising:

an execution pipeline;

cache memory coupled to the execution pipeline to hold processor instructions arranged in a software loop;

register rotation prediction hardware to predict physical register values for the processor instructions in future iterations of the software loop;

a software pipeline instruction buffer coupled between the execution pipeline and the register rotation prediction hardware to hold the processor instructions in future iterations of the software loop; and

at least one unarchitected frame marker register coupled to the register rotation prediction hardware to hold predicted register offsets for future iterations.

18. (Original) The processing system of claim 17 wherein the execution pipeline includes register renaming logic responsive to the at least one unarchitected frame marker register.

19. (Previously Presented) A processing system comprising:

an execution pipeline;

cache memory coupled to the execution pipeline to hold processor instructions arranged in a software loop;

register rotation prediction hardware to predict physical register values for the processor instructions in future iterations of the software loop;

a software pipeline instruction buffer coupled between the execution pipeline and the register rotation prediction hardware to hold the processor instructions in future iterations of the software loop; and

the register rotation prediction hardware includes a circuit to specify complete physical register addresses for the processor instructions in future iterations of the software loop.

20. (Original) The processing system of claim 19 wherein processor instructions held in the software pipeline instruction buffer include fully specified physical register addresses.

21. (Previously Presented) A processing system comprising:

an execution pipeline;

cache memory coupled to the execution pipeline to hold processor instructions arranged in a software loop;

register rotation prediction hardware to predict physical register values for the processor instructions in future iterations of the software loop;

a software pipeline instruction buffer coupled between the execution pipeline and the register rotation prediction hardware to hold the processor instructions in future iterations of the software loop; and

the execution pipeline is configured to speculatively execute instructions received from the software pipeline instruction buffer.

22. (Original) The processing system of claim 21 further comprising a plurality of unarchitected predicate registers, wherein the instructions within the software pipeline instruction buffer are predicated on at least one of the plurality of unarchitected predicate registers.

23. (Canceled)

24. (Canceled)

25. (Previously Presented) A method of executing a software pipelined loop comprising:

rotating registers for each iteration of the loop;

predicting register rotations for future iterations of the loop;

the software pipelined loop comprises at least one branch instruction, the method further comprising issuing at least one non-branch instruction simultaneously with the at least one branch instruction; and

the at least one non-branch instruction is predicated on an unarchitected predicate register.

26. (Previously Presented) A method of executing a software pipelined loop comprising:

rotating registers for each iteration of the loop;

predicting register rotations for future iterations of the loop;

the software pipelined loop comprises at least one branch instruction, the method further comprising issuing at least one non-branch instruction simultaneously with the at least one branch instruction; and

speculatively removing stop bits from the at least one branch instruction.

27. (Original) The method of claim 26 further comprising speculatively executing the at least one non-branch instruction.

28. (Previously Presented) A method of executing a software pipelined loop comprising:

rotating registers for each iteration of the loop;

predicting register rotations for future iterations of the loop;

responsive to a hint register, predicting register rotations for more than one iteration in the future; and

modifying at least one unarchitected frame marker register.

29. (Previously Presented) The method of claim 28 further comprising:

speculatively executing instructions for the more than one iteration in the future; and

squashing the speculative execution if a data dependence between loop iterations occurs incorrectly.

30. (Original) The method of claim 29 further comprising modifying the hint register when speculative execution is squashed.

31. (New) The processor of claim 3 further comprising speculation decision making hardware connected to the register rotation prediction unit to compute values for the plurality of unarchitected frame marker registers.

32. (New) The processor of claim 31 further comprising register renaming hardware in a pipeline, the register renaming hardware being responsive to the plurality of unarchitected frame marker registers.

33. (New) The processor of claim 4 further including a trace cache configured to hold prediction hint information for each trace.

34. (New) The processor of claim 33 further comprising a trace cache fill unit to apply register rotation prediction to traces as traces are constructed.

35. (New) The processing system of claim 17 further comprises speculation decision making hardware connected to the register rotation prediction unit to compute values for the at least one unarchitected frame marker register.

36. (New) The processing system of claim 19 further comprising fully specified physical register addresses for the processor instructions held in the software pipeline instruction buffer.

37. (New) The processing system of claim 21 further comprising a hint register to encode prediction hints for the register rotation prediction hardware.

38. (New) The method of claim 25 further including generating static hints for the predicting of register rotations.

39. (New) The method of claim 25 further including generating dynamic hints at runtime for the predicting of register rotations.

40. (New) The method of claim 26 further including generating dynamic hints for the predicting of register rotations.